Low noise divide by 2 circuit 24-10-2005

This document describes how to build a simple divider. It is intended as to widen the available XO clock frequencies at TentLabs. The circuit works well with all clocks, including 45.1584 MHz.

- Parts required
  L ferrite bead non polar
  C 10uF longest pin is +
  IC 74HC74 Dtype flipflop
  R 47 ohm All resistors

- Circuit diagram

![Circuit Diagram](image)

The flipflop gives a divide by 2 at both outputs Q and Q. Depending on the application, one of these can be taken (their phases differ 180 degrees)

- Building notes
  Mount the parts on a small universal vero-board. Take notes below into account. Tie non-used inputs of the IC (pins 10 to 13) to ground.

- Decoupling Notes
  Ensure good decoupling, at Tentlabs all necessary info can be found.

- Power supply notes
  In addition, a clean power supply is required. When TentLabs XO2/XO3 boards are used. Vcc can be tapped from L1. Depending on the project, 3.3V or 5.0V operation is required.

- Testing
  Assure the supply voltage is < 5.5V. Power the circuit and check (oscilloscope or counter) if the outputs generate the intended new clock.

- Divide / 4
  Obviously cascading 2 dividers will give a divide / 4 signal. The other half of the IC can be used, since the signals are synchronous (never mix a-synchronous signals in one IC). Check the datasheet for other inputs: 74HC74.

Suces !

Guido Tent