Supply decoupling and layout of circuits with digital ICs

As I am employed as an EMC engineer within Philips Semiconductors (Eindhoven, the Netherlands), and still an enthusiast (tube) audio-designer, I was happily surprised to read Jon Marks' article in the July issue of HiFi world in 1998. He describes how RFI (or RF emission) can influence hi-fi equipment's sound, and how screening can affect this RFI.
However as screening is only one part of the battle against RFI, I took this opportunity to write this article to point out some other issues that need attention when designing for low RFI.

In this contribution I would like to concentrate on the most important aspects of circuit and PCB layout. However I would like to mention some "general" aspects first.

1. Never use a higher bandwidth then strictly necessary. Whenever possible reduce currents and their frequency content (by adding local low-pass filtering)
2. Keep loops as small as possible
3. Consider that attached cables like for example mains, antenna, loudspeaker and SPDIF create the biggest loops and need little current to emit heavily
4. If available, choose SMD packages for ICs

Now let's look at supply decoupling.

The usual decoupling
In figure 1 a (sub) circuit, consisting of 2 ICs is depicted. Their respective decoupling capacitors are placed in vicinity, as we learned from most textbooks. In figure 2 the RF equivalent circuit is given.

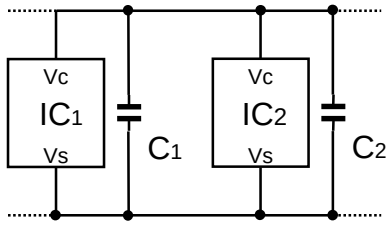

Figure 1: regular supply decoupling

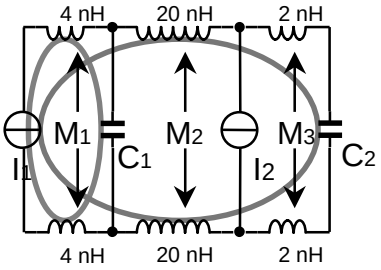

Figure 2: equivalent RF-circuit

The traces that interconnect the supply and reference of the ICs are replaced by inductances. These are weakly coupled as they might be on a double layer board with a ground plane (coupling ~ 0,8). As such both fluxes compensate partly. Due to this, an average inductance of 2 nH each cm (sorry, no inches here) can be assigned to the traces. As an example, average values are given in the figure. Normal DIL packages lead to such values.
Now we distinct two current loops. The smallest, with C1 inside, is intended to short the RF current of IC1. The bigger is hidden, and seldom considered. The supply lines and the capacitor C2, assigned to IC2, create this loop.

The impedances $j\omega L$ and $-j\omega C$ will be complex conjugate for a certain frequency f. With L = 44 nH and C = 100 nF we find f = 2.4 MHz. At this frequency the supply loop will resonate. As there are no or very small resistive elements in the LC network, a quality-factor of 100 can be expected. In this loop resonance currents will appear, 100 times bigger then generated inside the IC supply, will run. These currents do run in bigger loops than intended!
In an average application up to 10 ICs might be present. This might end in up to 100 loops, as all ICs have their own decoupling capacitor. All those loops will resonate at different frequencies, throughout a huge range. These resonance frequencies are defined by the physical structure of the PCB, and as such will all differ.

The given frequencies are no exceptions; in a multibit DA converter clocked at for example 11.2896 MHz, a spectrum starting at few 100 kHz up to at least 200 MHz can be found. 1- bit converters are even worse as they operate at higher (internal) clock frequencies.

The better decoupling
In figure 3 a suggestion is made to improve the decoupling.

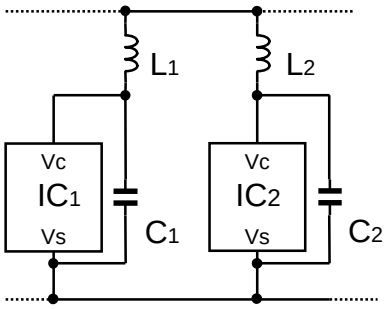

Figure 3: improved supply

At first inductances L1 and L2 (> 1 μH) are placed in every supply line of digital ICs, before they are connected to the power supply line(s). As a consequence the impedance towards the supply is dominated by L. The chance of a resonance still appears, but the frequency will be far lower than the aforementioned 2.4 MHz. As long as we use RF chokes as inductances, no damping of the circuit appears.

When lossy ferrite beads are applied, some damping is added as well. This can be seen when we consider the equivalent circuit of a bead, given in figure 4.

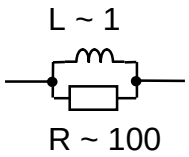

Figure 4: typical RF-equivalent of lossy ferrite bead

Ferrite has dissipative properties, represented by a resistor R. As such the Q of the decoupling circuit lowers significantly; resonances are well damped. For DC it behaves as a straight wire, so no voltage drop appears in the supply line. However, when the circuit consumes only few mA, a resistor can be applied as well, as this only gives a small voltage drop. A minimum value of 100 Ω is advised.
Suitable beads are available from Philips Murata and many others. Databooks in general clearly state the properties like impedance versus frequency and maximum DC current. Again a minimum of 100 Ω at 100 MHz can be taken as a rule of thumb. The final choice mainly depends on the frequencies that appear in your circuit. Consider at least 20 times the highest clock frequency.

The inductances must be placed closely to the IC, but their routing is far less critical as the decoupling capacitor placement and routing, as pointed out below.

Decoupling capacitor routing
The usual way capacitors C are connected to the reference is already shown out in figure 1. Usually when a ground plane is available they are connected by placement only; the ground is everywhere, one would say.
Minimising the loop area is most important, that is true. However, another, often forgotten, aspect must be taken into account. As can be seen in figure 2, inductances have been assigned to the ground plane as well. As the decoupling currents run through these inductances, they generate RF-voltages U = L (dI / dt) across the plane. These voltages will appear in series with the functional signals crossing this part of the plane. As such functional disturbance might appear within the system as these voltages may appear in series with functional signals on the PCB.

As a direct consequence the RF emission of the whole PCB increases as well as the RF voltage driving the attached cables increases.

The better way
The solution is within the connection and routing of the capacitor. The safest way is to place every decoupling capacitor as close as possible to the Vss (ground) pin(s) of the IC(s). As such only the smallest part of the groundplane will carry the decoupling current. Furthermore the routing of this capacitor to the Vcc (power) pin of the IC deserves careful attention.

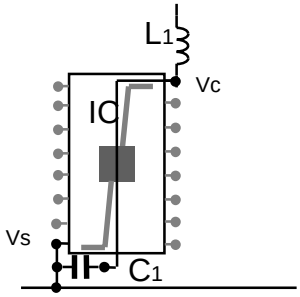

Figure 5: proper way to route the decoupling capacitor

As an illustration the layout of silicon (die, bondwires and leadframe) has been shown in grey. Now the route shown can be considered optimal; the current loop is minimal as it is following the internal current path. When we add the third dimension (height) it becomes clear why an IC socket is not favourable; the loop height will increase, and as such its' area.

ICs with more than one supply / ground pin
If an IC has more supply pins, every pin must be connected following the same strategy.

If an IC has more then one ground pin, for example an analogue and a digital ground, all must be connected directly to the first ground layer on the PCB, beneath the IC.

On chip decoupling
Some last generation ICs have a decoupling capacitor integrated on silicon. In this case no external capacitor shall be used. As the external capacitor always has lower impedance, the current again will run in the external capacitor loop, which is opposite to the intended.

The supply pin(s) of ICs with on chip decoupling capacitors must be connected directly with a ferrite bead. The decoupling strategy does not change; only the position of the capacitor does.

Decoupling capacitor quality

Very often two capacitors are connected in parallel; 100 nF ceramic and 4,7 µF for example. This habit originates from history. In the early years electrolytics had poor RF characteristics and a smaller ceramic or foil cap, with good RF behaviour, was placed in parallel. Figure 6 shows the equivalent of an electrolytic.

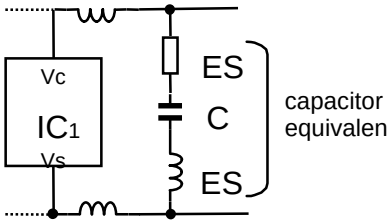

Figure 6: decoupling capacitor

Modern electrolytics are far better RF performers. Their construction is such that the series inductance is very low (both films are terminated at the same side). They have very low impedance over up to 4 decades in frequency; Enough to say goodbye to the additional ceramic capacitor. It saves money and space as well and eliminates the risk of yet another resonance.

When selecting an electrolytic, the series inductance must be taken into account, and properly compared to the total inductance of the supply loop the cap is in. That inductance of the (for a DIL28 package for example) is about 12 nH. The ESL of the capacitor shall be relatively small compared to this value; it does not make sense to look for 2 nH as the loop itself dominates!

The author has good experience with electrolytics of Philips series 179, Oscon SC-SA series and Black Gate FK-types, but many other electrolytics might meet your requirements as well.

Other current loops

Until now we only considered supply loops. As ICs need to interface, signal loops appear once we interconnect ICs. As some I/O buffers or “ordinary” inverters can drive up to tenths of mA, and we only need few to drive the next stage, a series resistor in the output is often added. Values of 47 Ω to 1 kΩ are applicable. Care must be taken that the minimum required signal-slope be maintained (as is necessary for example to maintain jitter specifications and or susceptibility levels). If we consequently add series resistors, a circuit similar to the one illustrated in figure 7 appears.

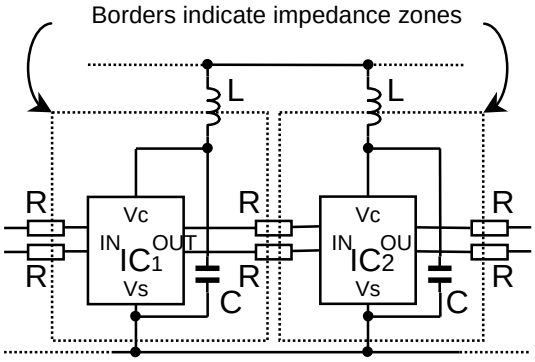

Figure 7: ICs interfacing

As an example 2 ICs are taken. In series with their in- and outputs resistors are inserted. Now restricted areas around each IC appear. I call these “impedance zones” as they are only crossed by impedances (> 100 Ω). The only hard (DC) connection is via the ground-plane. As Kirchoff still applies (sum of currents in and out an IC is zero) we now have full control over the RF current through the ground connection(s) of the IC (one exception here, that has to do with a parasitic current, described later).

Component placement
Most circuits consist of a multitude of active components. They are drawn as such, but it is not wise to put them on the PCB the same way. As an example a digital to analogue converter (DAC) is taken. This is a project that I am privately involved in, with three friends.

A DAC typically consists of an input receiver (IR) to recover clock and data, and a digital filter (DF) to achieve filtering in the digital domain. Furthermore there are two digital to analogue converter chips (DAC) that finally create an analogue signal out of the digital. Analogue lowpass filtering (LPF) finally follows. The analogue line stage consists of a tube configured as anode follower, but is not depicted here.

After extensive listening tests and measurements we found that the jitter of the recovered clock signal (from the input receiver) as well as the jitter at the outputs of the input receiver did not meet our requirements. As such, we added a phase locked loop (PLL) controlling a voltage controlled crystal oscillator (VCXO). On top of that we added re-clocking of all signals that enter the DA chips, in order to remove the internally generated jitter of the digital filter. The phase comparator (PC) is built from discrete logic, as we did not find existing integrated comparators good enough.

The PCB is separated in two areas: digital and analogue. The analogue part consists of the PLL loopfilter (LPF) and gain element (GAIN) and the input (control) terminal of the VCXO. Therefor the VCXO is placed across the border. The same holds for the LPF filter, filtering the output of the comparator; it has a digital input and an analogue output.

The DA-chip silicon is well laid out. After examining the pins and their functions, a straight line could be drawn through the chip, separating analogue from digital. Luckily the analogue and digital supply is separated as well (Burr Brown PCM63). As such, the placement of these DA chips becomes obvious and unique, as in drawing 8.

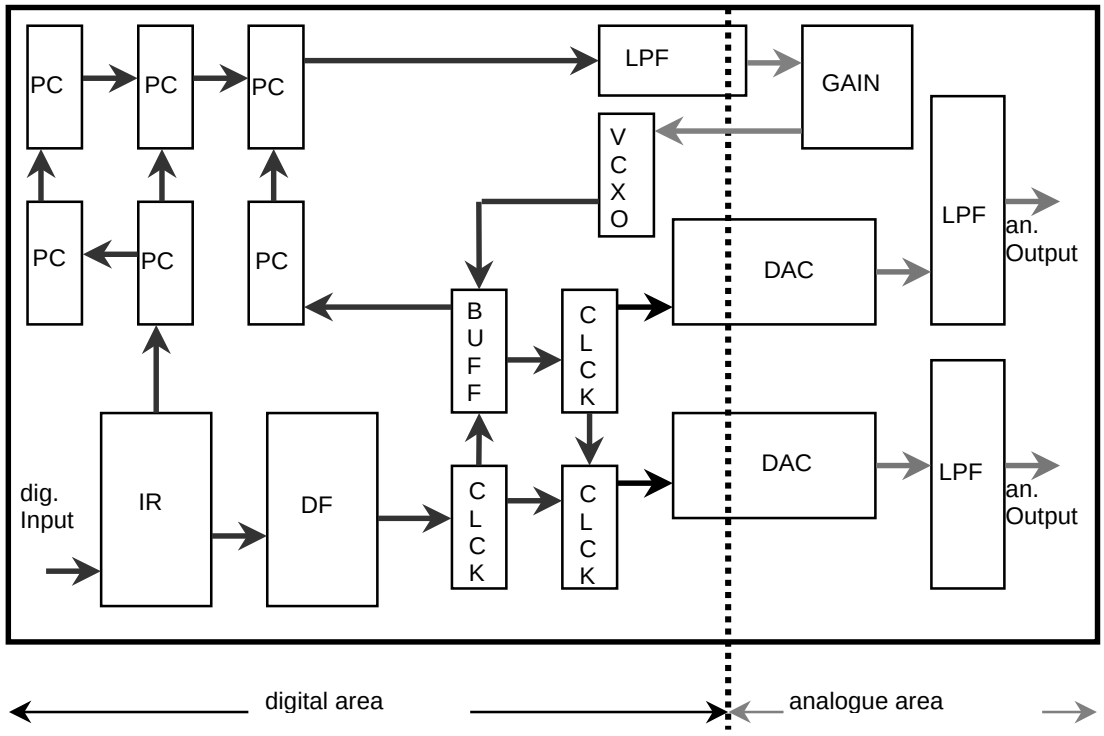

Figure 8: PCB floorplan of digital to analogue converter

The route dictated by the signal forces placement of all other chips. The phase comparator is planned in a corner, as it is a circuit with a lot of logic (6 ICs). If it were in the middle their voltage build-up in the groundplane could disturb others more. Finally all signals crossing from analogue to digital (drawn in grey) do so with a series impedance of 100 Ω or more.

Layers
With nowadays clock-speeds at least a double layer board must be used in order to meet European emission limits and to maintain signal integrity. We can assign one layer as a groundplane. This layer will be the closest to the ICs (component side) and act as an electrical screen as well. For high frequencies (practice shows > 200 MHz) the die of the IC starts acting as an electrical mono-pole. Reduction of this type of emission has been shown useful by Jon Marks' article.

With the described decoupling philosophy signals interacting between ICs will always run through the groundplane, regardless of the transaction (high to low or low to high). As the supply lines do no longer carry RF currents (at least, if you have followed the instructions in the first half of this article).

This enables us to create neat transmission lines between ground-plane and signal trace. Due to the use of series resistors and inductances, lots of bridges appear, effectively reducing the number of via's usually necessary.

Supply lines can be routed as a last step. Inductances have been added so the RF current through these lines is heavily reduced; their routing has become non-critical, as they only carry dc currents.

Never use power planes. It is not needed, as dc-supply currents only need small traces. A power plane may resonate with the groundplane: your PCB will act as dipole antenna!

Keep the groundplane closed
One final word to finish. Very often the groundplane is intersected by a slot, between the analogue and digital part of the PCB. The two planes are then connected beneath the AD or DA converter chip, or even worse at the supply-lines entry on the PCB (as advised by some IC manufacturers). With the planes separated, signal currents that cross the intersection are forced to return via the groundplane and as such need to describe a huge loop, around the intersection. This leads to high emission, and higher chance on inter-system pollution.

Recently a friend followed the measures described in this article, on a commercially available AD-converter (a demo board from a well-known manufacturer). Improvements finally decreased emission with 30 dB and enhanced both jitter and audio performance.

By taking appropriate measures, we know the whereabouts of amplitude, frequency-content and domain of the currents on the PCB. By shorting currents on a local basis, the currents through the plane are known as well the area they run in. We now can keep the plane closed and profit from all the advantages.

Link to tube amplifier wiring
The described philosophy can be applied to tube amps. Replace IC by gain stage (1 triode for example), ferrite beads can be read as filter choke or resistor (1 kΩ for instance) and the local decoupling capacitor is present as the already applied high voltage decoupling capacitor. Series resistance in signal lines is often present as the output impedance of gain stages is in the range of few kΩ. As such the reference or ground of the circuit only carries dc and can be made of thin wires.

The loop of rectifier and first capacitor carries higher (100 Hz) currents though. The ground path of this loop must never be part of the ground plane (as I have seen in commercially available amplifiers). That ground wiring must not be used in common (some share the ground with the heaters, yuck…….). Ground finally must be taken from the negative pole of the last supply capacitor (e.g. the output of a pi-filter) and fed into the circuit, starting with the output stage.

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Guido Tent, February 1999